ABSTRACT

A data processing apparatus maps input symbols to be communicated onto a predetermined number of carrier signals of an Orthogonal Frequency Division Multiplexed (OFDM) symbol. The data processor includes an interleaver memory which reads-in the predetermined number of data symbols for mapping onto the OFDM carrier signals. The interleaver memory reads-out the data symbols on to the OFDM carriers to effect the mapping, the read-out being in a different order than the read-in, and the order being determined from a set of addresses. The set of addresses are generated from an address generator. The address generator includes a linear feedback shift register and a permutation circuit.